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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Kie Y. Ahn et al.

Title: BIPOLAR TRANSISTORS WITH LOW-RESISTANCE EMITTER CONTACTS

Attorney Docket No.: 303.466US1

PATENT APPLICATION TRANSMITTAL

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BIPOLAR TRANSISTORS WITH LOW-RESISTANCE EMITTER CONTACTS

Background of the Invention

The present invention concerns integrated circuits, particularly fabrication methods, structures, and circuits for bipolar transistors.

Integrated circuits, the key components in thousands of electronic and computer products, are interconnected networks of electrical components fabricated on a common foundation, or substrate. Fabricators typically use various techniques, such as layering, doping, masking, and etching, to build thousands and even millions of microscopic transistors, resistors, and other electrical components on a silicon substrate, known as a wafer. The components are then "wired," or interconnected, together to define a specific electric circuit, such as a computer memory, microprocessor, or logic circuit.

Many integrated circuits include a common type of transistor known as a bipolar transistor or bipolar junction transistor. The bipolar transistor has three terminals, or contacts: a base, a collector, and an emitter. In digital integrated circuits, such as memories, microprocessors, and logic circuits which operate with electrical signals representing ones and zeroes, the bipolar transistor behaves primarily as a switch, with the base serving to open and close an electrical connection between its collector and emitter. Closing the switch essentially requires applying a certain current to the base, and opening it requires applying a reverse current.

One class of bipolar transistor problems concerns the structure, composition, and fabrication of its emitter contact. This contact is a highly conductive structure that facilitates electrical connection of the emitter region of the transistor to other parts of a circuit. Conventional emitter contacts are formed from polysilicon using a self-aligned bipolar technology, a simple fabrication technique which accurately aligns the polysilicon base and emitter contacts of bipolar transistors. The self-aligned bipolar technology is widely used not only because of its simplicity, but because it yields bipolar transistors with shallow emitters and bases which in turn

provide good switching speed and current gain. Yet, in looking to the future, the polysilicon emitter contacts, which have a higher than desirable electrical resistance, stand in the way of better switching speed and current gain ---two criteria important to the development of faster computers and other devices that use integrated circuits.

One promising solution to this problem is to form the emitter contact from a material with less resistance than polysilicon. For example, aluminum has about one-tenth the resistance of polysilicon. However, the 650°C melting temperature of aluminum is less than some temperatures inherent to the self-aligned bipolar technology. In particular, the conventional self-alignment technique includes outdiffusion and emitter-driving steps that require heating the emitter contact to 900-1000°C, which would undoubtedly melt an aluminum emitter contact.

Accordingly, there is a need not only for bipolar transistors with lower, emitter-contact resistance, but also for methods of making them.

Summary of the Invention

To address this and other needs, the inventors have developed bipolar transistor with low-resistance, aluminum, silver, and gold emitter contacts, as well as methods for making them. One method embodiment forms a conventional bipolar transistor with a polysilicon emitter contact, and then substitutes at least a portion of the polysilicon emitter contact with either aluminum, silver, or gold, to reduce its resistance and thereby provide superior switching speed and current gain.

In an exemplary embodiment, the substitution of aluminum for the polysilicon emitter contact entails depositing aluminum on the polysilicon contact and then annealing the resulting structure to urge cross-diffusion of the aluminum and the polysilicon. The cross-diffusion ultimately displaces substantially all of the polysilicon with aluminum, leaving behind a low resistance aluminum contact. Another facet of the invention include a heterojunction bipolar transistor with a low-resistance emitter contacts. And, still another is an integrated memory circuit which includes bipolar transistors with the low-resistance emitter contact.

Brief Description of the Drawings

Figure 1 is a cross-sectional view of an integrated-circuit assembly in fabrication;

Figure 2 is a cross-sectional view of the Figure 1 integrated-circuit assembly after opening a window 20 in layers 16 and 18;

Figure 3 is a cross-sectional view of the Figure 2 assembly after forming extrinsic base regions 22a-22b, hole 23, insulative sidewalls 24a and 24b, and intrinsic base region 26;

Figure 4 is a cross-sectional view of the Figure 3 assembly after forming a two-layer polysilicon structure comprising layers 28a and 28b;

Figure 5 is a cross-sectional view of the Figure 4 assembly after forming layers 32 and 34 on polysilicon structure 28;

Figure 6 is a cross-sectional view of the Figure 5 assembly after substituting metal from layer 32 with polysilicon structure 28 to produce a metal emitter contact 32'; and

Figure 7 is a block diagram of a generic dynamic-random-access-memory circuit that incorporates bipolar transistors having low-resistance emitter contacts according to the present invention.

Detailed Description of Preferred Embodiments

The following detailed description, which references and incorporates Figures 1-7, describes and illustrates specific embodiments of the invention. These embodiments, offered not to limit but only to exemplify and teach the invention, are shown and described in sufficient detail to enable those skilled in the art to practice the invention. Thus, where appropriate to avoid obscuring the invention, the description may omit certain information known to those of skill in the art.

Exemplary Fabrication Method and Structure
for Bipolar Transistor with Low-Resistance Emitter Contact

Figures 1-6 show a number of exemplary integrated-circuit assemblies, which taken collectively and sequentially illustrate the exemplary method of making a bipolar transistor with a low-resistance emitter contact. In particular, Figures 1-3 depict part of a conventional method of making a standard double-polysilicon, self-aligned bipolar transistor, and Figures 4-6 illustrate an extension to the process that ultimately yields an exemplary structure for a bipolar transistor which has a metal emitter contact, and therefore provides a lower emitter resistance and higher current gain than conventional bipolar transistors which have polysilicon emitter contacts.

More specifically, as shown in Figure 1, the conventional process begins with an n-type silicon substrate 12. The term "substrate," as used herein, encompasses a semiconductor wafer as well as structures having one or more insulative, semi-insulative, conductive, or semiconductive layers and materials. Thus, for example, the term embraces silicon-on-insulator, silicon-on-sapphire, and other advanced structures.

The method then forms a buried collector 14 and local oxidation regions 15a and 15b in substrate 12. Local oxidation preferably follows a LOCOS isolation process. Afterward, the method grows or deposits a heavily p-type doped (P+) polysilicon layer 16 on the substrate. Polysilicon layer 16 may be doped during the deposition (in situ) or through an implantation procedure after deposition. An insulative layer 18, such as silicon dioxide, is then deposited or grown on polysilicon layer 16.

In Figure 2, the method opens a window 20 through insulative layer 18 and polysilicon layer 16, exposing a portion of underlying substrate 12 and thus defining an active region 20a of substrate 12. This procedure, which entails etching through layers 16 and 18 down to substrate 12, effectively divides polysilicon layer 16 into left and right segments 16a and 16b that will serve as base contacts. As known in the art, the position of window 20 is important to the self-alignment of the base and emitter contacts. If the overlap of segments 16a and 16b with the active region 20a

is too large, the resulting bipolar transistor will suffer from an overly large base-collector capacitance and a consequent reduction of switching speed. On the other hand, if the overlap is too small, the resulting transistor will be fatally flawed, since inevitable lateral encroachment of oxide regions 15a and 15b will eliminate the base contact with region 20a and thwart transistor operation.

In Figure 3, the method outdiffuses extrinsic base 22a and 22b from polysilicon segments 16a and 16b. As known in the art, this is a high temperature procedure generally requiring temperatures in the range of 900-1000°C. After this, an insulative layer 24 is grown or deposited on segments 16a-16b and active region 20a, and subsequently etched back to substrate 12, leaving oxide sidewall spacers 24a and 24b and a hole 23. The method then implants, through hole 23, an intrinsic p-type base region 26 between extrinsic bases 22a and 22b.

The conventional method would next entail forming a heavily n-type doped (n+) polysilicon emitter contact within hole 23 and then out-diffusing some of the n+ dopant into base region 26 to form an n+ emitter region. However, in contrast to this conventional approach which yields a polysilicon emitter contact having higher-than-desirable emitter contact resistance, the exemplary method, as Figure 4 shows, forms a two-layer polysilicon structure 28 in hole 23, comprising a metal-diffusion-barrier layer 28a on base region 26 and a doped polysilicon layer 28b on barrier layer 28a. After forming n+ emitter region 30 in base region 26 through out-diffusion as would the conventional process, the method substitutes metal for at least a portion of polysilicon layer 28b to form a low-resistance emitter contact 32'.

More specifically, after forming hole 23 and sidewall spacers 24a and 24b, the exemplary method forms diffusion barrier layer 28a in hole 23 on emitter region 28. Layer 28a is preferably 200-300 Angstroms thick and comprises heavily n-type doped (n+) polysilicon carbide (SiC), with 50 percent carbon. In other embodiments, diffusion barrier layer 28a consists of microcrystalline silicon carbide, polycrystalline silicon oxycarbide, titanium nitride, amorphous silicon, or other suitable metal-diffusion-barring material.

After formation of diffusion layer 28a, the method forms polysilicon layer 28b with a silane precursor to a desired thickness of 500 nanometers. In the exemplary embodiment, layers 28a and 28b are formed in a continuous polysilicon deposition procedure, initially depositing polysilicon with a carbon additive to form layer 28a and subsequently discontinuing the additive to form layer 28b. For further details on the formation of the exemplary diffusion barrier, refer to H. Moller, et al., "In-situ P- and N- Doping of Low-Temperature Grown Beta-SiC Epitaxial Layers on Silicon," (Proceedings of International Conference on Silicon Carbide and Related Materials, pp. 497-500, 1996. IOP Publishing, United Kingdom) which is incorporated herein by reference. In addition, see Z. A. Shafi et al., "Poly-crystalline Silicon-Carbide (SiCarb) Emitter Bipolar Transistors," IEEE Bipolar Circuits and Technology Meeting, Minneapolis, MN pp. 67-70, 1991, which is also incorporated herein by reference.

Next, the method substitutes metal, preferably an aluminum alloy, for polysilicon layer 28b to form metal emitter contact 32'. Figure 5 shows that, in the exemplary embodiment, this entails forming a one-half-micron-thick metal layer 32, consisting of an aluminum alloy having 0.3-4.0 percent copper and 0.3-1.6 percent silicon, over polysilicon layer 28b by a deposition technique such as evaporation or sputtering. The method then entails formation of a 0.1-0.2 micron-thick, titanium layer 34 on metal layer 32, again preferably using a deposition technique. In other embodiments, layer 34 is between 20 and 250 nanometers thick and comprises zirconium or hafnium, instead of titanium. Layer 34, which is optional, reduces the temperature and time necessary to complete the next step, which forces a metal-substitution reaction between metal layer 32 and polysilicon layer 28b.

To force this reaction between aluminum and polysilicon, the exemplary method heats, or anneals, the integrated-circuit assembly to 450°C in a nitrogen, forming gas, or other non-oxidizing atmosphere for approximately 60 minutes. Heating urges diffusion of metal layer 32 into polysilicon layer 28b and vice versa, ultimately substituting polysilicon layer 28b with metal from metal layer 32, an aluminum alloy in the exemplary embodiment. This substitution process is bounded

at the interface of polysilicon layer 28b and metal-diffusion barrier 28a. The annealing process yields a superficial by-product of polysilicon and titanium silicide. Removing the by-product by chemical mechanical polishing or other suitable planarization techniques leaves a metal emitter contact 32', as shown in Figure 6.

Other embodiments of the bipolar transistor and fabrication method form emitter contact 32' from metals other than the exemplary aluminum alloy. For example, other embodiments form the emitter contact from more conductive, but costlier metals, such as gold and silver. In these embodiments, layer 28b comprises a polycrystalline silicon-germanium alloy with 10 to 60 percent germanium.

These embodiments require different annealing temperatures to effect the metal substitution reaction. In general, the annealing, or substitution, temperature should not exceed the eutectic temperature of the metallic system comprising metal layer 32 and layer 28b. To form a gold gate contact one would form layer 32 from gold and anneal at approximately 300°C, and to form a silver gate contact one would form layer 32 from silver and anneal at approximately 500-600°C. These embodiments also use zirconium, which has a lower solubility than titanium and hafnium in silver and gold, to form optional layer 34.

Changing the composition of layer 28b will also affect the annealing temperature. For example, layer 28b may comprise polysilicon and germanium, not just polysilicon. In the aluminum embodiment, this change reduces the anneal temperature to approximately 400°C, instead of 450°C.

In addition, other embodiments omit barrier layer 28a. In contrast to the exemplary embodiment where this layer not only prevents diffusion of emitter metal into base and emitter regions 26 and 30, but also facilitates control of the metal-substitution process, embodiments lacking barrier layer 28a are somewhat less reliable and more difficult to make.

Furthermore, the methods described above to fabricate a bipolar transistor with a metal emitter contact are useful to form silicon-germanium (SiGe) heterojunction bipolar transistors suitable for RF wireless applications. In RF applications, reducing emitter resistance to avoid emitter degeneration and its

attendant current-gain reductions is generally more important than in other applications, such as digital memory and logic circuits. These SiGe heterojunction transistors are similar in structure and composition to assembly 10, except that base region 26 consists of a uniform or graded silicon-germanium $Si_{1-X}Ge_X$ composition, where x is a variable. For the graded base composition, x varies with depth, preferably increasing with distance from emitter 30.

Exemplary Embodiment of an Integrated Memory Circuit Incorporating the Bipolar Transistor with Low-Resistance Emitter Contact

Figure 7 shows one example of the unlimited number of applications for transistors having the low-resistance emitter structure of the present invention: a generic integrated memory circuit 40. Memory circuit 40 includes a number of subcircuits, which comprise one or more bipolar transistors. More precisely, circuit 40 includes a memory array 42 which comprises a number of memory cells 43, a column address decoder 44, and a row address decoder 45, bit lines 46, word lines 47, and voltage-sense-amplifier circuit 48 coupled in conventional fashion to bit lines 46.

In the exemplary embodiment, each of the memory cells, the address decoders, and the amplifier circuit includes one or more bipolar transistors that has the low-resistance emitter structure of the present invention. However, in other embodiments, only one of the components, for example, memory array 42 or voltage-sense-amplifier circuit 48, includes bipolar transistors with the low-resistance emitter structure. Circuit 40 operates according to well-known and understood principles.

Conclusion

The present invention provide practical structures, fabrication methods, and circuits for bipolar transistors with low-resistance emitter contacts of aluminum, silver, gold, or other metals. One method embodiment forms a polysilicon emitter contact self-aligned with polysilicon base contacts and then replaces or substitutes at

least a portion of the polysilicon emitter contact with aluminum, not only forming a low-resistance aluminum contact, but also precluding exposure of the aluminum contact to the aluminum-melting temperatures occurring during emitter and base formation.

The embodiments described above are intended only to illustrate and teach one or more ways of practicing or implementing the present invention, not to restrict its breadth or scope. The actual scope of the invention, which embraces all ways of practicing or implementing the invention, is defined only by the following claims and their equivalents.

What is claimed is:

1. A method of making an emitter contact for an emitter region of a bipolar transistor, the method comprising:

forming a polysilicon structure on an emitter region position; and

substituting metal for at least a portion of the polysilicon structure.

2. The method of claim 1 further including forming an emitter region at the emitter region position after forming the polysilicon structure.

3. The method of claim 2 wherein the polysilicon structure includes a doped layer and forming the emitter region comprises outdiffusing dopant from the doped layer to the emitter region position.

4. The method of claim 1, wherein forming the polysilicon structure on an emitter region position comprises:

forming a diffusion barrier layer; and

forming a polysilicon layer on the diffusion barrier layer.

5. The method of claim 4, wherein the diffusion barrier layer comprises at least one of the following: a silicon carbide, a silicon oxycarbide, and a titanium nitride.

6. The method of claim 4, wherein the polysilicon layer includes polysilicon and germanium.

7. The method of claim 1 wherein substituting metal for the polysilicon structure comprises substituting metal for substantially all of the polysilicon structure.

8. The method of claim 1 wherein substituting metal for at least a portion of the polysilicon structure, comprises:

depositing metal on the polysilicon structure; and

urging diffusion of the deposited metal into the polysilicon structure.

9. The method of claim 8, wherein urging diffusion of the deposited metal and the polysilicon structure comprises heating the deposited metal and the polysilicon structure.

10. The method of claim 1 wherein substituting metal for at least a portion of the polysilicon structure comprises:

forming a metal layer on the polysilicon structure; and

heating the metal layer and the polysilicon structure.

11. The method of claim 1 wherein the metal comprises at least one of aluminum, gold, and silver.

12. A method of making an emitter contact for a bipolar transistor, the method comprising:

forming a polysilicon structure on a layer of the transistor, the polysilicon structure including:

a diffusion barrier layer on the layer; and

a polysilicon layer on the diffusion barrier layer; and

substituting metal for at least a portion of the polysilicon layer.

13. The method of claim 12, wherein the polysilicon layer includes a dopant.

14. The method of claim 12, wherein the diffusion barrier layer comprises at least one of the following: a silicon carbide, a silicon oxycarbide, and a titanium nitride, and the polysilicon layer includes polysilicon and germanium.

15. The method of claim 12 wherein substituting metal for the polysilicon layer comprises substituting metal for substantially all of the polysilicon layer.

16. The method of claim 12 wherein substituting metal for at least a portion of the second polysilicon layer, comprises:

depositing metal on the polysilicon layer; and

heating the deposited metal and the polysilicon layer.

17. The method of claim 12 wherein the metal comprises at least one of aluminum, gold, and silver.

18. A method of making an emitter contact for a bipolar transistor, the method comprising:

forming a polysilicon structure on a layer of the transistor, the polysilicon structure including a doped diffusion barrier layer on the layer and a polysilicon layer on the diffusion barrier layer;

depositing metal including at least one of aluminum, gold, and silver on the polysilicon layer; and

heating at least the deposited metal and the polysilicon structure to urge diffusion of the deposited metal into the polysilicon layer.

19. The method of claim 18, wherein the diffusion barrier layer comprises at least one of the following: a silicon carbide, a silicon oxycarbide, and a titanium nitride.

20. A method of making a metal contact for a bipolar transistor, the method comprising:

forming a polysilicon structure on a layer of the transistor; and

substituting metal for at least a portion of the polysilicon structure.

21. The method of claim 20 further including forming an emitter region in the layer underneath and in contact with the polysilicon structure.

22. The method of claim 21 wherein the polysilicon structure includes a doped layer contacting a region of the layer and forming the emitter region comprises diffusing dopant from the doped layer into the region.

23. A method of making a bipolar transistor having self-aligned base contacts and self-aligned metal emitter contact, the method comprising:

forming first and second polysilicon base contacts on a semiconductive layer, the contacts spaced apart to define an active region in the semiconductive layer;

outdiffusing dopant from the first and second base contacts into the semiconductive layer to form extrinsic base regions aligned with the base contacts;

implanting an intrinsic base region in the active region;

forming a doped polysilicon structure on the intrinsic base region;

forming an emitter region self-aligned with the doped polysilicon structure by outdiffusing dopant from the doped polysilicon structure into the intrinsic base region; and

substituting metal for at least a portion of the polysilicon structure after forming the emitter region, thereby forming a metal emitter contact self-aligned with the emitter region.

24. The method of claim 23:

wherein the polysilicon structure includes:

a doped diffusion barrier layer on the intrinsic base region; and

a polysilicon layer on the doped diffusion barrier layer; and

wherein substituting metal for at least a portion of the polysilicon structure includes substituting metal for substantially all of the polysilicon layer.

25. The method of claim 24, wherein the diffusion barrier layer comprises at least one of the following: a silicon carbide, a silicon oxycarbide, and a titanium nitride, and the polysilicon layer includes polysilicon and germanium.

26. The method of claim 24 wherein substituting metal for substantially all of the polysilicon layer comprises:

depositing metal on the polysilicon layer; and

heating at least the deposited metal and the polysilicon layer to a predetermined temperature.

27. The method of claim 23 wherein the metal comprises at least one of aluminum, gold, and silver.

28. A method of reducing emitter resistance of a bipolar transistor, the method comprising:

forming a bipolar transistor structure having a polysilicon emitter contact;

substituting metal for at least a portion of the polysilicon emitter contact.

29. A silicon-germanium (SiGe) heterojunction bipolar transistor for RF wireless applications, the transistor comprising:

a diffusion barrier layer contacting an emitter region and comprising at least one of the following: a silicon carbide, a silicon oxycarbide, and a titanium nitride;

a metal layer contacting the diffusion barrier layer and comprising at least one of aluminum, gold, and silver; and

a SiGe base region contacting the emitter region;

30. The SiGe heterojunction bipolar transistor of claim 29 wherein the base region has a graded silicon-germanium $Si_{1-X}Ge_X$ composition, where x varies according to position along a depth dimension of the base region.

31. An integrated memory circuit comprising:

a memory array having a plurality of memory cells;

an address decoder coupled to the memory cells;

a plurality of bit lines coupled to the memory cells;

a voltage-sense-amplifier circuit coupled to the bit lines; and

wherein at least one of the memory cells and the voltage-sense amplifier circuit includes a bipolar transistor comprising:

a diffusion barrier layer contacting an emitter region and comprising at least one of the following: a silicon carbide, a silicon oxycarbide, and a titanium nitride; and

a metal layer contacting the diffusion barrier layer and comprising at least one of aluminum, gold, and silver.

Abstract of the Disclosure

Many integrated circuits include a type of transistor known as a bipolar junction transistor, which has an emitter contact formed of polysilicon. Unfortunately, polysilicon has a relatively high electrical resistance that poses an obstacle to improving switching speed and current gain of bipolar transistors. Current fabrication techniques involve high temperature procedures that melt desirable low-resistance substitutes, such as aluminum, during fabrication. Accordingly, one embodiment of the invention provides an emitter contact structure that includes a polysilicon-carbide layer and a low-resistance aluminum, gold, or silver member to reduce emitter resistance. Moreover, to overcome manufacturing difficulties, the inventors employ a metal-substitution technique, which entails formation of a polysilicon emitter, and then substitution of metal for the polysilicon.

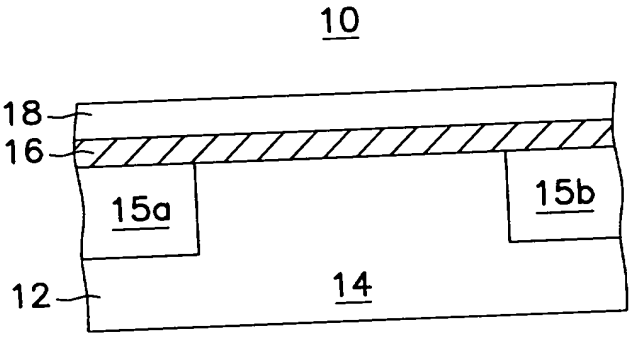


FIG. 1

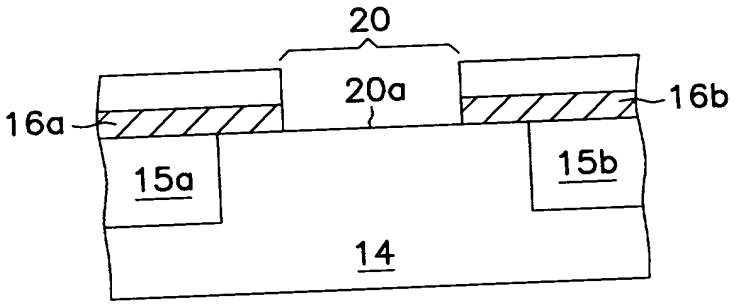


FIG. 2

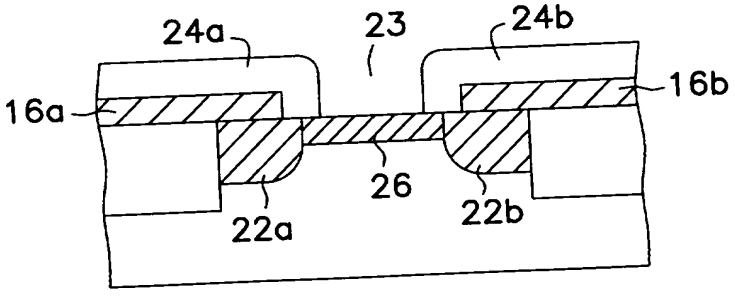


FIG. 3

FIG. 4

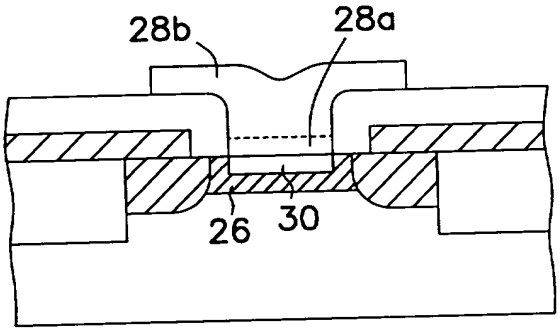


FIG. 5

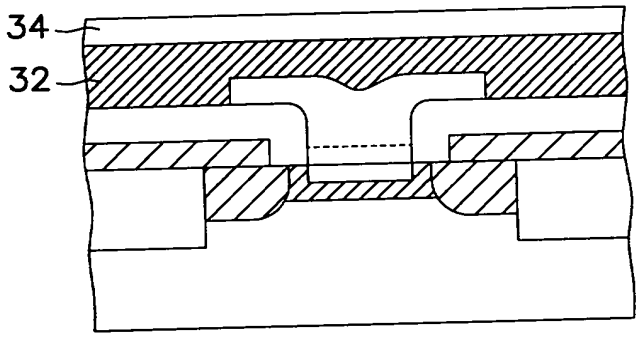
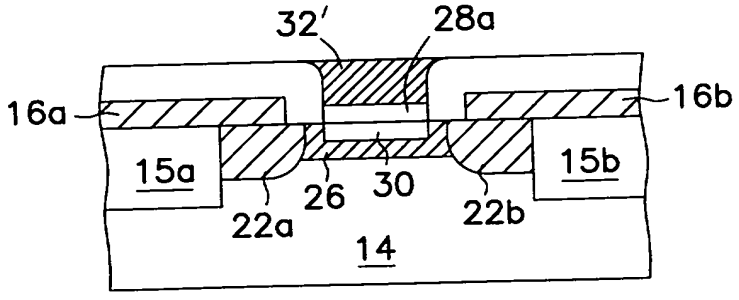


FIG. 6



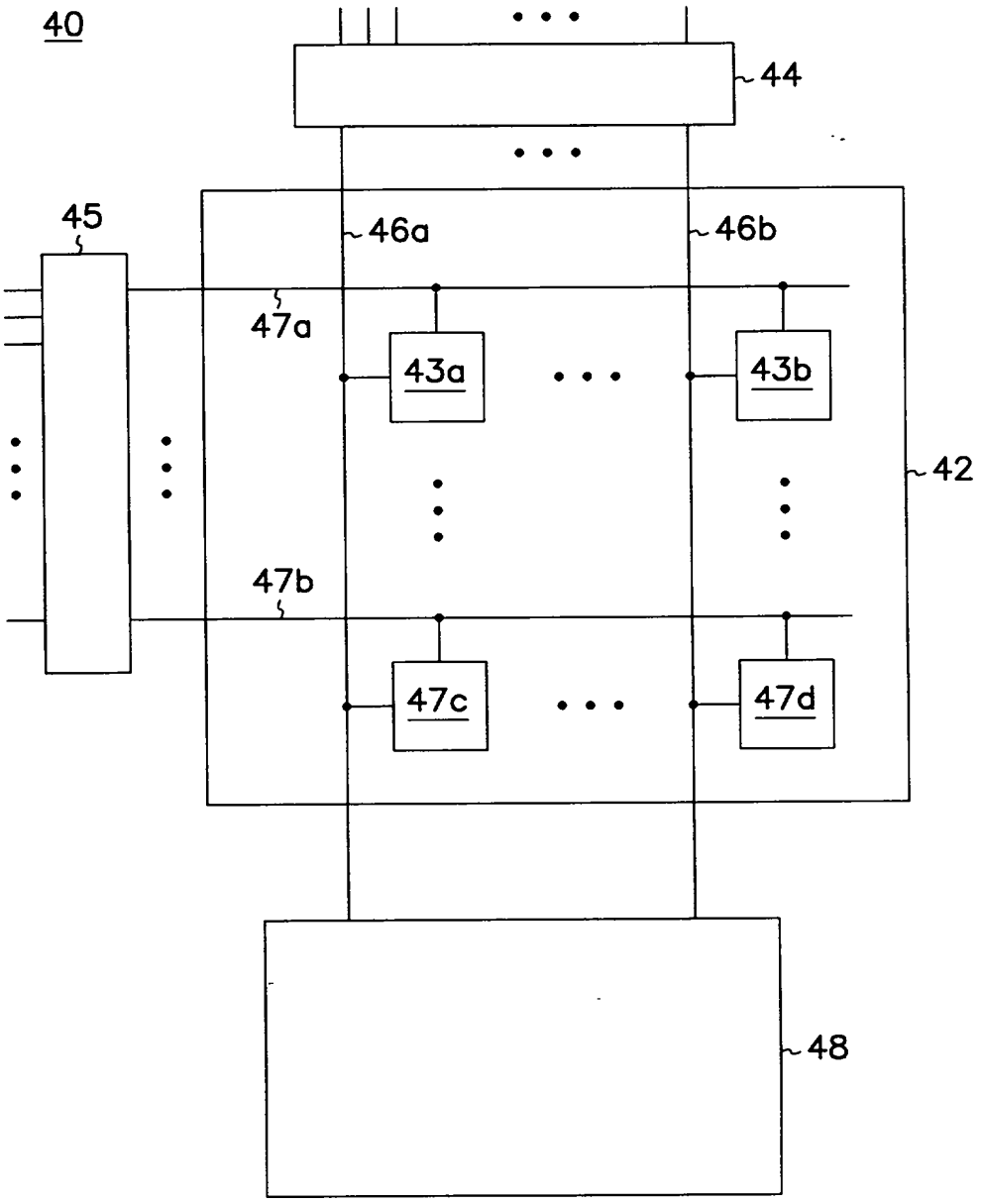


FIG. 7

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Serial No.:	Unknown	Group Art Unit: Unknown	
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Title:	BIPOLAR TRANSISTORS WITH LOW-RESISTANCE EMITTER CONTACTS		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. listed as follows:

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Clark, Barbara J	Reg No 38,107	Kluth, Daniel J.	Reg. No. 32,146	Taylor, Michael W.	Reg. No. P-43,182
Drake, Eduardo E	Reg. No. 40,594	Lemaire, Charles A.	Reg. No. 36,198	Viksnins, Ann S.	Reg. No 37,748
Dryja, Michael A.	Reg. No. 39,662	Litman, Mark A.	Reg. No. 26,390	Woessner, Warren D.	Reg. No. 30,440
Embretson, Janet E.	Reg. No. 39,665				

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia M. Pappas (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

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Dated: April 27, 1998

MICRON TECHNOLOGY, INC.

By: _____

Name: Michael L. Lynch

Title: Chief Patent Counsel

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first an joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

BIPOLAR TRANSISTORS WITH LOW-RESISTANCE EMITTER CONTACTS .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such applications have been filed.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

No such applications have been filed.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such applications have been filed.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of joint inventor number 1 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: Kie Y. Ahn Date: Kie Y. Ahn apr. 24, 1998
Kie Y. Ahn

Full Name of joint inventor number 2 : **Leonard Forbes**
Citizenship: **United States of America** Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: _____
Leonard Forbes

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first an joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

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Corvallis, OR 97330

Signature: _____ Date: 27 APR 98
Leonard Forbes

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

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Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

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